REMARKS:

Applicant appreciates the thorough examination of the application that is reflected in the Office Action dated August 12, 2003. Applicant rewrites claims 2 and 16 in independent form. The scope of claims 2 and 16 has not changed as a result of these amendments. Applicant also changes the dependency of claims 3 and 17 such that those claims now depend from independent claims 2 and 16, respectively. Claims 2, 3 and 5-18 are pending in the application. Reexamination and reconsideration of the application are respectfully requested.

Art-based Rejections

The Office rejects claims 1-2, 4-8, 12 and 18 under 35 U.S.C. 102(e) as being anticipated by Shimizu (USPN 5,801,674), rejects claims 3 and 17 under 35 U.S.C. 103(a) as being unpatentable over Shimizu further in view of Yasunishi (USPN 6,094,243), and rejects claims 9-11 and 13-15 under 35 U.S.C. 103(a) as being unpatentable over Shimizu further in view of S-MOS System Inc., Dot Matrix liquid crystal display Driver SED 1520/21 Version 1.0 (October, 1996) (hereinafter S-MOS).

Applicant respectfully traverses these rejections for at least the following reasons.

Claims 1 and 4

Applicant respectfully submits that the cited references fail to teach or suggest, for example, "wherein the master IC has an output terminal for outputting the display control signal from the display control signal generation section of the master IC," or "wherein each of the master IC and the at least one slave IC has an input terminal which is connected to the output terminal of the master IC," as required by claims 1, 4.

Applicant respectfully submits that according to the Shimizu reference neither the master IC nor the slave IC's have an input terminal (such as those identified in Fig. 1 of the present application by reference numerals 130 and 184) for receiving the display control signal output from the display control signal generation section of the master IC. *(See Shimizu Fig. 1; Fig. 2).* In particular, the master IC (3) of Shimizu does not have an input terminal (such as that identified in Fig. 1 of the present application by reference numeral 130) for inputting a display control signal from the display control signal generation section of the master pattern IC (3). *(See id)*

Moreover, as shown in Figs. 1 and 2 of Shimizu, the slave IC's (5,6) of Shimizu are not connected the master IC (3).

Accordingly, the Shimizu reference fails to teach or suggest, " wherein the master IC has an output terminal for outputting the display control signal from the display control signal generation section of the master IC," or "wherein each of the master IC and the at least one slave IC has an input terminal which is connected to the output terminal of the master IC," as required by claims 1,4.

Accordingly, Applicant respectfully submits that claims 1 and 4 are patentable over the cited Shimizu reference.

Claims 2 and 16

Applicant respectfully submits that the cited references fail to teach or suggest, for example, "a display address circuit which assigns a display address for the display data which is read out from the display memory and displayed in the display section," or that "the display control signal input through the input terminal is supplied to the display address circuit and the driver," as required by claim 2.

At page 2 and 3 of the Office Action, the Office asserts that the data register 15 of Shimizu corresponds to the claimed "display memory," that the liquid crystal

display driving circuit 17 of Shimizu corresponds to the claimed "driver," and that the cascade connection control circuit 12 of Shimizu generates "a display control signal." In the paragraph bridging pages 3-4 of the Office Action, however, the Office does not explain where the Shimizu reference teaches a "display address circuit." As shown in FIG. 2 of the Shimizu reference, the output of the cascade connection control circuit 12 is provided only to the output terminal EO and the sequence control circuit 13. As discussed at col. 4, lines 61-64 of the Shimizu reference, the "data fetch starting signal and load signal which the sequence control circuit 13 outputs to control the data register 15 and output latch 16 are generated in the cascade connection control circuit by decoding the SYNC signal." Therefore, the sequence control circuit 13 of Shimizu is not a "display address circuit," nor does it assign "a display address for the display data which is read out from the display memory," as required by claim 2.

Thus, Applicant respectfully submits that the cited references fail to teach or suggest at least the above recitations of claim 2. Accordingly, Applicant respectfully submits that claim 2 is patentable over the cited references. In addition, Applicant respectfully submits that dependent claim 3 is separately patentable at least by virtue of its dependency from independent claim 2. Applicant further submits that independent claim 8, 12, and 16 are patentable for at least the same reasons, and that dependent claims 9-11; 13-15 ; and 17 are patentable at least by virtue of their dependency from independent claims 8, 12, and 16, respectively.

Claims 5 and 7

Applicant respectfully submits that the cited references fail to teach or suggest, for example, "an internal delay circuit which delays the display control signal," or "an output terminal which outputs the display control signal before the display control signal passes through the internal delay circuit," as required by

claim 5. In rejecting claims 5 and 7, pages 2 and 3 of the Office Action are silent with respect to these limitations. Moreover, as shown in FIG. 2 of the Shimizu reference, the output of the cascade connection control circuit 12 is provided only to the output terminal EO and the sequence control circuit 13. As such, Shimizu does not suggest , "an internal delay circuit which delays the display control signal," as required by claim 5. Moreover, the output terminal EO in Shimizu does not output "the display control signal before the display control signal passes through the internal delay circuit," as required by claim 5. There nothing in Shimizu that even remotely suggests this feature of claim 5.

Thus, Applicant respectfully submits that the cited references fail to teach or suggest at least the above recitations of claim 5. Accordingly, Applicant respectfully submits that claim 5 is patentable over the cited references. In addition, Applicant respectfully submits that dependent claim 6 is separately patentable at least by virtue of its dependency from independent claim 5, and also because claim 6 requires additional features that are not disclosed or suggested by the cited references. For example, the Shimizu reference also do not suggest that "the signal delay in the internal delay circuit is variable," as required by claim 6.

Applicant further submits that independent claim 7 is patentable for at least the same reasons as claim 5, and that dependent claim 18 is patentable at least by virtue of its dependency from independent claim 7, and also for at least the reasons discussed above with respect to claim 6.

Claims 8 and 12

As noted above independent claims 8 and 12 are patentable for the same reasons discussed with respect to claims 2 and 16. In addition, Applicant respectfully submits that claims 8 and 12 are also patentable over the Shimizu reference since the Shimizu reference also fails to teach or suggest, for example, "a selection terminal for selecting either a master or a slave," and "an input terminal

to which the display control signal is input from an external device," as required by claims 8 and 12.

In rejecting claim 8, the Office Action asserts at pages 2-3 that the liquid crystal display driving circuit 17 of Shimizu corresponds to the claims "driver," that the output terminal EO corresponds to the claimed "output terminal," and that the input terminal EI corresponds to the claims "input terminal." The Office Action is silent with respect to where the Shimizu reference teaches the claimed "selection terminal for selecting either a master or a slave." For at least this reason, the rejection of claims 8 and 12 should be withdrawn.

As shown in FIG. 2 of Shimizu reference, the liquid crystal display driving circuit 17 has two inputs – a first input from the sequence control circuit 13 and a display data input from the output latch 17. However, the Office Action takes the position that the cascade connection control circuit 12 generates "a display control signal." The input terminal EI of Shimizu does not receive the output signal from the cascade connection control circuit 12, as required by claims 8 and 12. Moreover, the input terminal EI of Shimizu does not receive the output signal from the cascade connection control circuit 12 "from an external device," as required by claims 8 and 12. Thus, the Shimizu reference also fails to teach or suggest, for example, "an input terminal to which the display control signal is input from an external device," as required by claims 8 and 12.

Thus, Applicant respectfully submits that the cited references fail to teach or suggest at least the above recitations of claims 8 and 12. Accordingly, Applicant respectfully submits that claims 8 and 12 patentable over the cited references. In addition, Applicant respectfully submits that dependent claims 9-11 and 13-15 are separately patentable at least by virtue of its dependency from independent claims 8 and 12, and also because those claims require additional features that are not disclosed or suggested by the cited references.

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In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6809 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

Date: January 12, 2004

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